Amendments to the Specification:

Please replace the paragraph beginning on page 2, line 5 with the following amended paragraph:

As shown in Figure 1, a low K dielectric layer 20 is formed above a semiconductor 10. Although omitted from the Figure, any number of intervening layers can be formed between the semiconductor 10 and the dielectric layer 20. In some cases a barrier layer 30 is formed on the low K dielectric layer 20. Most high performance integrated circuits use copper to form the metal interconnects. Copper lines are typically formed using a damascene-type process in which a trench is first formed in the dielectric. The trenches are then filled with copper using a copper electroplating process. As shown in Figure 1, trenches 34 ~~36~~, 36 are formed in the dielectric layer 20. A lined layer 40 is formed in the trench prior to the formation of the copper lines. The liner typically comprises tantalum nitride or other similar material. The low K dielectric material used to form the dielectric layer 20 is a porous material and typically comprises an open pore structure. During the formation of the liner layer 40, the material used to form the liner layer 40 will penetrate into the low K dielectric material resulting in the formation of regions of liner material 50 in the low K dielectric material 20. Following the formation of the liner layer 40, the trenches 34, 36 are filled with copper 45 to form the interconnect lines. In the case of adjacent trenches it is possible that the liner material can form a path 60 that connects the trenches. If the liner material is electrically conductive then an electrical short will exist between the copper lines in the adjacent trenches. This electrical short can cause the integrated circuit to malfunction or cease to operate.